IN THE CLAIMS

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Claim 1. (Currently amended) A method of supporting programs that include instructions that modify subsequent instructions in a processor system with a storage controller and a central processing unit including an execution unit, an instruction unit, and a plurality of caches including separate instruction cache and operand cache, the method comprising:

subjecting said instruction cache and said operand cache of said central processing unit to a cache coherency protocol with interlocks on cache block access including:

allowing shared read access by said instruction cache and said operand cache to a cache block if said cache block has read only status in said instruction cache and said operand cache;

allowing read and write access by said operand cache and preventing access by said instruction cache to said cache block if said cache block has exclusive status in said operand cache; and

interlocking access to said cache block by said operand cache with exclusive status in said operand cache if said cache block has already~~been accessed~~ ~~by~~read-only status in said instruction cache.

Claim 2. (Original) The method of Claim 1 further including interfacing said cache coherency protocol with said storage controller employing a processor system cache coherency protocol.

Claim 3. (Original) The method of Claim 2 further including interfacing said cache coherency protocol with existing cache handling requirements.

Claim 4. (Original) The method of Claim 1 further including interfacing said cache coherency protocol with existing cache handling requirements.

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Claim 5. (Currently amended) The method of Claim 3 further including:

buffering a ~~register of~~ cache block addresses in a register-file~~locations~~ in said instruction cache corresponding to~~for~~ fetched unexecuted instructions in an instruction buffer in said instruction unit;

when data is required to be stored or updated, evaluating a cache block's status for a desired storage address in said operand cache and transmitting a request for exclusive status to said storage controller and transmitting a cross interrogate signal to said instruction cache;

allowing an operand store once exclusive status is obtained from said storage controller and a response from said cross interrogate signal;

discarding and refetching data in said instruction cache if ~~said~~ an associated cache block in said instruction cache matches said desired storage address;

when instruction fetch is requested, providing said instruction cache read-only status for a requested cache block;

discarding and refetching data in said instruction buffer and re-buffering cache locations in said register if an instruction stream of said execution unit changes; and

discarding data in said instruction buffer and discarding said cache locations in said register if said execution unit completes execution of fetched instructions.

Claim 6. (Original) The method of Claim 5 further including discarding and refetching data in said instruction cache and in said instruction buffer, and discarding and re-buffering said cache locations in said register, if said cache handling requirements dictate.

Claim 7. (Currently amended) The method of Claim 5 wherein said exclusive status is obtained by:

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following said request for exclusive status, said storage controller invalidates exclusive status for said requested cache block at any other place within said processor system; and

following said request for exclusive status, said storage controller invalidates read-only status for said requested cache block at any other place within said processor system, including said central processing unit making said request.

Claim 8. (Currently amended) The method of Claim 5 wherein said instruction cache responds to said cross interrogate signal by:

generating a response to ~~said probe and~~ said cross interrogate signal and a hit signal indicative of an address match if said desired storage address matches an associated cache block in said instruction cache and if a location of said associated cache block matches any valid entry in said register, otherwise responding with a no hit signal; and

invalidating said associated cache block in said instruction cache if said desired storage address matches.

Claim 9. (Original) The method of Claim 5 wherein said instruction cache includes cache locations in said register corresponding to said fetched unexecuted instruction addresses.

Claim 10. (Original) The method of Claim 5 wherein said cache handling requirements are an existing protocol that dictates when least recently utilized data in cache be replaced.

Claim 11. (Currently amended) The method of Claim 5 wherein said cross interrogate signal is employed to support probing a directory in said ~~I-~~instruction cache with said desired storage address.

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Claim 12. (Original) The method of Claim 11 wherein said directory and said registers comprises six cache locations.

Claim 13. (Currently amended) The method of Claim 1 wherein said shared read access implies that both instruction and operand cache may read a target cache block.

Claim 14. (Original) The method of Claim 1 wherein said exclusive status dictates sole update access to a target cache block anywhere in said processor system.

Claim 15. (Original) The method of Claim 1 wherein read-only status dictates that said cache block is not held with exclusive status anywhere in said processor system.

Claim 16. (Currently amended) The method of Claim ~~1~~ 2 wherein said processor system may be a multi-processor system including a plurality of central processing units.

Claim 17. (Currently amended) The method of Claim 16 wherein said -processor system cache coherency protocol is an existing protocol that allows said central processing unit to share access to cache blocks with other central processing units of said plurality of central processing units in said processor system.

Claim 18. (Original) A system for supporting programs that include instructions that modify subsequent instructions in a processor system said system comprising:

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a storage controller;

a central processing unit including an execution unit, an instruction unit, and a plurality of caches including separate instruction cache and operand cache;

said central processing unit coupled to said storage controller;

said execution unit coupled to said instruction unit, said instruction cache and said operand cache;

said instruction unit coupled to said instruction cache and said operand cache;

said instruction cache coupled to said operand cache; and

said processor system subjecting said instruction cache and said operand cache of said central processing unit to a cache coherency protocol with interlocks on cache block access.

Claim 19. (Currently amended) The system of Claim 18 wherein said subjecting includes:

said storage controller allowing shared read access by said instruction cache and said operand cache to a cache block if said cache block has read only status status in said instruction cache and said operand cache;

said storage controller allowing access by said operand cache and preventing access by said instruction cache to said cache block if said cache block has exclusive status in said operand cache; and

said storage controller interlocking read and write access to said cache block by said operand cache with exclusive status in said operand cache if said cache block has read-only status in ~~already been accessed by~~ said instruction cache.

Claim 20. (Currently amended) The system of Claim 19 wherein said subjecting further includes ~~includes~~ said storage controller interfacing said cache coherency protocol with a processor system cache coherency protocol.

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Claim 21. (Original) The system of Claim 20 wherein said subjecting further includes said storage controller interfacing said cache coherency protocol with existing cache handling requirements.

Claim 22. (Original) The system of Claim 21 wherein said cache handling requirements are an existing protocol that dictates when least recently utilized data in cache be replaced.

Claim 23. (Original) The system of Claim 19 wherein said subjecting further includes said storage controller interfacing said cache coherency protocol with existing cache handling requirements.

Claim 24. (Currently amended) The system of Claim 22 further including:

said instruction cache buffering a ~~register of~~ cache block addresses in a register-file~~locations for~~ corresponding to fetched unexecuted instructions in an instruction buffer in said instruction unit;

when data is required to be stored or updated, evaluating a cache block's status for a desired storage address in said operand cache and transmitting a request for exclusive status to said storage controller and transmitting a cross interrogate signal to said instruction cache;

allowing an operand store once exclusive status is obtained from said storage controller and a response from said cross interrogate signal;

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discarding and refetching data in said instruction cache if ~~said~~ an associated cache block in said instruction cache matches said desired storage address;

when instruction fetch is requested, providing said instruction cache read-only status for a requested cache block;

discarding and refetching data in said instruction buffer and re-buffering cache locations in said register if an instruction stream of said execution unit changes; and

discarding data in said instruction buffer and discarding said cache locations in said register if said execution unit completes execution of fetched instructions.

Claim 25. (Original) The system of Claim 24 further including said instruction cache discarding and refetching data in said instruction cache and said instruction buffer, and discarding and re-buffering said cache locations in said register, if said cache handling requirements dictate.

Claim 26. (Currently amended) The system of Claim 24 wherein said exclusive status is obtained by:

said storage controller, following said request for exclusive status, invalidating exclusive status for said requested cache block at any other place within said processor system; and said storage controller, following said request for exclusive status, invalidating read-only status for said requested cache block at any other place within said processor system, including said central processing unit making said request.

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Claim 27. (Currently amended) The system of Claim 24 wherein said instruction cache responds to said cross interrogate signal by:

generating a response to ~~said probe and~~ said cross interrogate signal and a hit signal indicative of an address match if said desired storage address matches an associated cache block in said instruction cache and if a location of said associated cache block matches any valid entry in said register, otherwise responding with a no hit signal; and

invalidating said associated cache block in said instruction cache if said desired storage address matches.

Claim 28. (Original) The system of Claim 24 wherein said instruction cache includes cache locations in said register corresponding to said fetched unexecuted instruction addresses.

Claim 29. (Currently amended) The system of Claim 24 wherein said cross interrogate signal is employed to support probing a directory in said ~~I-~~instruction cache with said desired storage address.

Claim 30. (Original) The system of Claim 29 wherein said directory and said registers comprises six cache locations.

Claim 31. (Currently amended) The system of Claim 18 wherein said shared read access implies that both instruction and operand cache may read a target cache block.

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Claim 32. (Original) The system of Claim 18 wherein said exclusive status dictates sole update access to a target cache block anywhere in said processor system.

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Claim 33. (Original) The system of Claim 18 wherein read-only status dictates that said cache block is not held with exclusive status anywhere in said processor system.

Claim 34. (Currently amended) The system of Claim ~~18~~ 20 wherein said processor system may be a multi-processor system including a plurality of central processing units.

Claim 35. (Original) The system of Claim 34 wherein said processor system cache coherency protocol is an existing protocol that allows said central processor to share access to cache blocks with other central processing units of said plurality of central processing units in said processor system.